

ABSTRACT

A method for reducing the drain resistance of a drain-extended MOS transistor in a semiconductor wafer,
5 while maintaining a high transistor breakdown voltage. The method provides a first well (502) of a first conductivity type, operable as the extension of the transistor drain (501) of the first conductivity type; portions of the well are covered by a first insulator (503) having a first
10 thickness. A second well (504) of the opposite conductivity type is intended to contain the transistor source (506) of the first conductivity type; portions of the second well are covered by a second insulator (507) thinner than the first insulator. The first and second
15 wells form a junction (505) that terminates at the second insulator (530a, 530b). The method deposits a photoresist layer (510) over the wafer, which is patterned by opening a window (510a) that extends from the drain to the junction termination. Next, ions (540) of the first conductivity
20 type are implanted through the window into the first well; these said ions have an energy to limit the penetration depth (541) to the first insulator thickness, and a dose to create a well region (560) of high doping concentration adjacent to the junction termination (530a).